

REMARKS

Claim 1 calls for each of said processors to have a different instruction set than the other processors. "Said processors" include a mathematical processor, an input processor, an output processor, and a master processor.

The material relied upon in the office action teaches away from the claimed invention. Specifically, the material relied on at column 14, line 47, is explicit that only two different types of processors are utilized. Thus, rather than teaching a different instruction set for each processor, the cited reference teaches making all the processors one of two types, either the type used for the master processor or the type used for the other processors.

The material cited with respect to the input processor (column 14, line 47 through column 15, line 18) does not in any way indicate that its instruction set is different from anything else. It has certain functions to do, but nothing in this material indicates that it uses a different instruction set than what all the other processors use. To the contrary, as suggested in the material relied on in column 14, only two different types of systems are utilized.

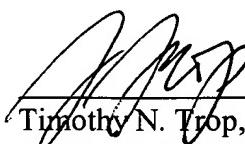
Similarly, the material with respect to the output processor does not indicate that different instruction sets are utilized and doing so would be inconsistent with the material relied upon in column 14, line 47.

Moreover, no effort is made to indicate that the mathematical processor has a different instruction set than the input or output processors.

In short, the cited reference teaches away from the claimed invention and explicitly fails to teach all the limitations claimed.

Therefore, reconsideration would be appropriate.

Respectfully submitted,



Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.

1616 South Voss Road, Suite 750
Houston, TX 77057-2631
713/468-8880 [Phone]
713/468-8883 [Fax]
Attorneys for Intel Corporation

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